## REMARKS

The Communication mailed June 4, 2002, in connection with the above-identified application, is noted. This Communication indicates that the Amendment filed April 15, 2002 was not fully responsive "because [Applicants] failed to amend the Application in such a way that ALL the reference numbers that are in the drawings appear in the specification". No specific indication is given as to the reference numbers that are missing. In this regard, see 35 USC 132.

In any event, Applicants have further amended their specification in order to provide further correspondence between the reference numbers in the drawings and reference numbers in the specification of the above-identified application. The amendments made for correspondence have been provided in light of reference characters in U.S. Patent No. 6,114,753, issued September 5, 2000, which issued from the parent application of the above-identified application, Serial No. 08/857,674, filed May 16, 1997.

Noting particularly U.S. Patent No. 6,114,753, it is respectfully submitted that the present amendments to the specification do not add new matter to the application.

Moreover, upon further review of the drawings in the above-identified application, it was noted that in the various parts of Fig. 2 (that is, (2-a), (2-b) and (2-c)), reference character 2.6, for the pad on the semiconductor element, was omitted from the drawing figures. Accordingly, by a separate, concurrently filed, Second Request for Approval of Drawing Amendments, Applicants are requesting amendment of Fig. 2 to indicate pad 2.6.

In view of the present amendments to the specification and further in view of

the concurrently filed Second Request for Approval of Drawing Amendments, it is respectfully submitted that a complete response to the Office Action mailed January 14, 2002, has now been filed. Moreover, it is also noted that in the Office Action mailed January 14, 2002, all pending claims (that is, claims 1-18) were allowed. In view of the foregoing, continued allowance of claims 1-18, and passing of the above-identified application to issue in due course, are respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification by the current Supplemental Amendment. This marked-up version is on the attached pages, the first page of which is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 503.35443VX1) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please delete the paragraph added to page 8, after line 1, in the Amendment filed April 15, 2002, and add the following new paragraph on page 8, after line 1, as follows:

Fig. 9 shows a semiconductor device with a three layer structure for the adhesive layer. Shown is core layer (e.g., porous supporting layer) 10 with adhesive layers 20,20 on opposite sides of the core layer 10. Semiconductor chip 50 is provided on a semiconductor supporting substrate [90] (not shown). Lead 60, including wiring 40, is electrically connected to external connecting terminal 80 and electrode 100 of chip 50. External connecting terminal 80 is electrically connected to lead 60 via a hole in polyimide film 30. Sealing material 70 covers lead 60.

Please delete the paragraph on page 8, lines 6-18, from the Amendment filed April 15, 2002, and substitute therefor the following new paragraph:

The process can be divided into three representative sections. The first one, including STEPS 1-5 [(Fig. 2a)] (2-a), is a method for fabricating a semiconductor element comprising (1) the step 1 of applying an adhesive film 2.2 to the tape 2.1 having a pattern layer and a wire 2.1.2 to the tape 2.1, (2) the step 2 of adhering the tape 2.1 having a pattern layer to the semiconductor element 2.3 having the pad 2.6 by means of the adhesive film 2.2 while maintaining an insulating condition therebetween, (3) the step 3 of electrically connecting the pattern layer formed on

the tape 2.1 and the pad 2.6 on the semiconductor element 2.3, via connecting lead 2.1.1', formed from wire 2.1.1, (4) the step 4 of sealing the electrically connected portion with an insulating agent (e.g., mold resin) 2.4, and (5) the step 5 of forming an external terminal 2.5 on the tape for connection to the mounting substrate.

Please delete the paragraph bridging pages 8 and 9, from the Amendment filed April 15, 2002, and substitute therefor the following new paragraph:

The second one, including STEPS 6-10 [(FIG. 2b)] (2-b), is a method for fabricating a semiconductor element comprising (1) the step 6 of applying an adhesive film 2.2 to the semiconductor element 2.3 having pad 2.6, (2) the step 7 of adhering the tape 2.1 having a pattern layer to the semiconductor element 2.3 by means of the adhesive film 2.2 while maintaining an insulating condition therebetween, and adhering wire 2.1.1 to tape 2.1, (3) the step 8 of electrically connecting the pattern layer formed on the tape 2.1 and the pad 2.6 on the semiconductor element 2.3 via connecting lead 2.1.1', formed from wire 2.1.1, (4) the step 9 of sealing the electrically connected portion with an insulating agent 2.4, and (5) the step 10 of forming an external terminal 2.5 on the tape 2.1 for connection to the mounting substrate.

Please delete the paragraph on page 9, lines 12-23, from the Amendment filed April 15, 2002, and substitute therefor the following new paragraph:

The third one, including STEPS 11-14 [(Fig. 2c)] (2-c), is a method of

fabricating a semiconductor element comprising (1) the step 11 of setting the tape 2.1 having the pattern layer in registration and adhering the tape 2.1 to the semiconductor element 2.3 having pad 2.6, using the adhesive film 2.2 simultaneously with maintaining an insulating condition therebetween, and adhering wire 2.1.1 to tape 2.1, (2) the step 12 of electrically connecting the pattern layer formed on the tape 2.1 and the pad 2.6 on the semiconductor element 2.3 via connecting lead 2.1.1', formed from wire 2.1.1, (3) the step 13 of sealing the electrically connected portion with an insulating agent 2.4, and (4) the step 14 of forming an external terminal 2.5 on the tape 2.1 for connection to the mounting substrate.

Please delete the paragraph bridging pages 11 and 12, from the Amendment filed April 15, 2002, and substitute therefor the new paragraph:

Fig. 4 shows an example of the composition of a circuit tape to which an adhesive film is attached. The circuit tape 4.1 can be adhered to the semiconductor element 4.3. If a thermosetting resin is used for the adhesive layer 4.2 at the circuit tape side and a thermoplastic resin is used for the adhesive layer [4.3] (not shown in Fig. 4) at the side adhered to the semiconductor element, the circuit tape having the adhesive ability shown in Fig. 4 can be provided readily. Wire 4.1.1 is electrically connected to circuit tape 4.1.

Please delete the paragraph bridging pages 20 and 21, and substitute therefor the following new paragraph:

An epoxy group adhesive film 6.2 (see Fig. 6-1) (made by Hitachi Chemical Co., Ltd., AS 3000, 50 $\mu$m thick) was registered, placed, and adhered between a semiconductor element 6.3 and circuit tape 6.1 at 170°C for one minute with a pressure of 50 kgf/cm$^2$, and was then post-cured at 180°C for 60 minutes in a constant temperature bath. Subsequently, connecting leads on the circuit tape were electrically connected to pads of the semiconductor element by single point bonding. The connecting portion was encapsulated with an epoxy encapsulant 6.4 (made by Hitachi Chemical Co., Ltd., RC021C). Finally, the semiconductor device shown in Fig. 6-1 was obtained by fixing the solder balls, which were connecting terminals 6.5 with the mounting substrate, onto the circuit tape 6.1.

Please delete the paragraph bridging pages 21 and 22, and substitute therefor the following new paragraph:

A film material 6.2 (see Fig. 6-2) having a three layer structure was obtained by applying an adhesive agent (made by Hitachi Chemical Co. Ltd., DF335), composed of a die bonding film material, onto both surfaces of a polyimide film (made by Ube Kosan Co., Ltd., SGA, 50 $\mu$m thick) to a thickness of 50 $\mu$m. The obtained film material 6.2 was registered and adhered to circuit tape 6.1 at 170°C for five seconds with a pressure of 30 kgf/cm$^2$. Under the above conditions, the unadhered adhesive layer exhibited a sufficient adhesive force to adhere to the semiconductor element 6.3. The circuit tape attached with the film material was adhered to the semiconductor element at 200°C for one minute with a pressure of

30 kgf/cm$^2$, and was then post-cured at 200°C for 60 minutes in a constant temperature bath. Subsequently, connecting leads on the circuit tape 6.1 were electrically connected to pads of the semiconductor element by gang bonding. The connecting portion was encapsulated with an epoxy encapsulant 6.4 (made by Hitachi Chemical Co., Ltd., RC021C). Finally, the semiconductor device shown in Fig. 6-2 was obtained by fixing the solder balls, which served as connecting terminals 6.5 with the mounting substrate, onto the circuit tape 6.1. Also shown in Fig. 6-2 is outer frame 6.6.

Please delete the paragraph bridging pages 22 and 23, and substitute therefor the following new paragraph:

A low elastic adhesive film 6.2 composed of an epoxy resin and acrylic rubber (made by Hitachi Chemical Co. Ltd., trial product, 150 $\mu$m thick) was registered, placed, and adhered between the semiconductor element 6.3 and the circuit tape 6.1 at 180°C for 30 seconds with a pressure of 100 kgf/cm$^2$, and was then post-cured at 180°C for 60 minutes in a constant temperature bath. Subsequently, connecting leads on the circuit tape were electrically connected to pads of the semiconductor element by wire bonding. The connecting portion was encapsulated with a silicone encapsulant 6.4 (made by Toshiba Silicone Co., Ltd., TSJ 3150). Finally, the semiconductor device shown in Fig. 6-3 was obtained by fixing the solder balls, which served as connecting terminals 6.5 with the mounting substrate, onto the circuit tape 6.1. Also shown in Fig. 6-3 is outer frame 6.6.